REMARKS

Claims 1-6 remain pending in the application. The specification and claims 1-2 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

A number of the drawings were objected to as failing to comply with 37 C.F.R. §1.84(p)(5) because they allegedly include reference signs not mentioned in the description.

With respect to the letter "H" found in Figure 13, the Office's attention is directed to the specification at page 18, lines 21-24 which reads "In step H, a transaction grant message is ... ." As the reference character in question (i.e., "H") is in fact referred to in the specification, no change is believed to be required.

As to the remaining reference characters identified in the Action, Applicants have now corrected the informality by amending the specification to mention the reference characters. No new matter has been introduced.

The drawings were further objected to as failing to comply with 37 C.F.R. §1.84(p)(4) because reference character "A" has been used to designate both "start" in Figure 13 and "assign initial stack positions" on page 17, lines 23-25; because reference character "B" has been used to designate both "assign initial stack positions" in Figure 13 and "receive respective transaction requests" on page 17, lines 30-32; and because reference character "C" has been used to designate both "receive transaction request" in Figure 13 and "determine highest priority level" on page 18, lines 3-7.

In response, Applicants note that when comparison is made with the corresponding description from page 17, line 23 to page 18, line 9, it is evident that the discrepancies that form the bases for these objections have arisen in the description rather than in the drawings. In particular, step A has been incorrectly identified as "assign initial stack positions" rather than "Start" and this has upset the referencing to subsequent stages B and C, whereas reference to step D has been inadvertently omitted altogether. Thus, instead of amending Figure 13 (which is believed to be correct), Applicants consider it more appropriate to correct the description as follows:

On page 17, line 23, immediately before the first sentence, beginning "The initial set up of the arbitration scheme ...", the following sentence has been added: "The arbitration scheme starts at step A."

On page 17, lines 23-24, the sentence has been amended to read: "The initial set up of the arbitration scheme is to arrange the modules into initial stack positions (step [[A]] B) which are stored in the stack storage means 26."

On page 17, lines 30-32, the sentence has been amended to read as follows: "In step [[B]] C, the arbitration unit 21 receives respective transaction requests from any number of the modules M1 to M5."

And, on page 18, line 9, before the sentence beginning "The control means then masks ..." the following sentence has been inserted: "In step D, the control means obtains the highest priority transaction request."

With these amendments, all reference characters appearing in the figures are also believed to be mentioned in the specification, and the reference characters used in Figure 13 are believed to be compatible with their use in the description. Accordingly, it is respectfully requested that the objections to the figures under 37 C.F.R. §§ 1.84(p)(4)-(5) be withdrawn.

Claim 2 stands rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. This rejection is respectfully traversed.

The Office has rejected claim 2 on the grounds that there is no clear antecedent basis for the limitation "transaction buses" in line 14 of the claim and it is not clear whether the "transaction buses" are the same as the "transaction control buses" of lines 12-13. These buses are indeed the same. The more consistent terminology used throughout the specification is "transaction bus." Consequently, to address the Office's concern claim 2 has been amended by removing the word "control" from the third line of claim 2, so that the phrase "wherein the bus architecture has separate read, write and transaction *control* buses" (emphasis added) now reads "wherein the bus architecture has separate read, write and transaction buses."

In view of the above, claim 2 is believed to define the claimed subject matter with sufficient particularity and distinctness to satisfy the terms of the statute. Accordingly, it is respectfully requested that the rejection of claim 2 under 35 U.S.C. §112, second paragraph, be withdrawn.

Claims 1-4 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Number 5,925,118 to Revilla et al. ("Revilla"). This rejection is respectfully traversed.

In addressing this rejection, it is, first, informative to see how Applicants' specification describes the dual arbitration facility claimed in claim 1. Turning to pages 20-

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23 and related Figures 20-22, an arbitration unit has an initiation part 32, which controls access of a requested ("initiation" or launching) transaction, and a retirement part 33, which controls access of a return (sometimes called retirement, as here) transaction. The two parts are connected via read, write and transaction buses to a plurality of modules making up the processor.

When an initiation request is made, the initiation arbiter controls access to the read and write buses as appropriate, depending on the type of transaction. Any arbitration method can be used to implement this control. It is clear from page 21 that mature data may be returned at any arbitrary time, as disclosed in lines 18-20 of page 21. As also made clear in lines 21-22 of page 21, the initiation and return arbiters operate independently. The principal advantage of this is that the buses can be more fully utilized. Thus, as described, vacant clock cycles associated with a write transaction can be used to issue a read transaction on the transaction bus. This is also illustrated in Figure 21.

The present invention therefore utilizes an initiation arbiter for controlling transactions launched onto the bus architecture and a return arbiter for return transactions received over the bus architecture, the arbiters operating independently of one another. To even more clearly define this, claim 1 has been amended to define "the first and second arbiter means operating independently of one another."

Revilla fails to anticipate independent claim 1 at least because it neither discloses nor even suggests this feature. Figure 1 of Revilla shows two master modules M0 and M1 (20, 22) and two slave modules S0 and S1 (26, 28). The modules are inter-connected by separate address bus 30, write bus 32, read bus 34 and TQuals bus 36, which carries information about the transactions. The slaves are connected to the masters by an arbiter 24 which, as shown, communicates with all the read, write, address and TQuals buses connecting to the masters.

The description of the operation of the arbiter 24 is far from clear but it seems that operations initiated by a master are arbitrated on a priority basis before being sent to the slaves. There are only clues to what happens next. For instance, column 6, line 49 to column 7, line 10 says that the slave checks that it is the correct address for the transaction but does not send an acknowledgement to the master until the slave has completed a current operation. When it does send an acknowledgement, it is sent via the arbiter to the master. Column 6, lines 11-15 merely state that buses and control signals carry out the same functions between masters and arbiter as between slaves and arbiter.

Looking more closely at Figure 1 of Revilla, it is clear that there are no "requests" in respect of data returned from the slaves to the masters. Without these, it is not possible for there to be any arbitration in the return direction. So, although the return transactions appear to pass through the box 24 labeled "arbiter", there is actually no arbitration of return transactions. Moreover, from a consideration of the timing diagrams of Figures 2 and 3, and from the flow chart of Figure 4, it is clear that the operation of the arbiter in the initiating direction is related to the operation in the return direction, whereas in presently claimed embodiments the initiating and return arbitration functions are independent of one another, as just discussed.

In support of its rejection, the Office cites the passage in Revilla at column 3, lines 20-26 as being particularly relevant. However, this passage merely states that independent read and write buses can carry data at the same time as one another. The passage has nothing to do with whether initiating and return arbiters operate independently of one another. To the contrary, the passage at column 9, lines 52-65 seems to suggest that in fact the arbiter only operates on requests from the master function and these are on a simple priority basis.

For at least the foregoing reasons, it is therefore respectfully submitted that Revilla does not disclose or suggest the variously claimed embodiments defined by claim 1, or by any of the claims 2-4 which each depend from claim 1. Accordingly, it is respectfully requested that the rejection of claims 1-4 under 35 U.S.C. §102(e) be withdrawn.

Claim 5 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Revilla in view of U.S. Patent Number 4,094,000 to Brudevold ("Brudevold"). Claim 6 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Revilla in view of U.S. Patent Number 5,924,926 to Brown ("Brown"). In view of the above submissions regarding novelty of claim 1, it is believed that the rejection of claim 5 for being obvious relative to Revilla and Brudevold, and the rejection of claim 6 for being obvious relative to Revilla and Brown, are moot and that no further arguments need be presented. It is therefore respectfully requested that the rejections of claims 5 and 6 under 35 U.S.C. §103(a) be withdrawn.

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The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,

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